REMARKS

This paper is submitted in response to the Office Action for the above-identified application mailed June 18, 2003.

In the Office Action, Claims 2, 10 and 14 were rejected under 35 U.S.C. Sec. 103 for being unpatentable over Schilling (U.S. Pat. No. 6 236 405) in view of Winser (GB Pub. No. 2 240 016). Claims 3-6 and 11-13 were rejected for being obvious over the above combination further in view of Fowler (U.S. Pat. No. 6 339 428).

Independent Claims 8 and 9 were rejected under the above statute for being an obvious variation over what is taught by Fowler.

Initially, under cover of this Response, minor amendments are made to the specification and drawings. These changes do not introduce new matter into this application.

A replacement Abstract is provided.

Claims 3, 4, 6 and 8-14 are amended. Claims 2 and 5 are cancelled. New Claims 15-24 are added. Claims 8, 9, 10 and 14 remain the independent claims. Claims 3, 4, 6, 11-13 and 15-20 are dependent from Claim 10. Claims 21-24 are dependent from Claim 14. No claims are dependent from Claims 8 or 9.

Schilling is primarily directed to a means of performing bilinear filtering. The data used to perform this filtering is stored in a cache 614. The data used to perform the filtering are retrieved by a color extract unit 618.[1]

Schilling states that his assembly can be used to perform trilinear filtering. However, in order to perform this filtering Schilling states, "In this instance, the cache should be duplicated for the other level of detail."[2] If one has to duplicate the cache, one also has to duplicate the assembly for writing data into the cache and the assembly for extracting data from the cache.

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[1] U.S. Patent No. 6 236 405, column 7, lines 37-55.
[2] U.S. Patent No. 6 236 405, column 7, lines 58-60.

Williams is directed to a "parallel structure so that all eight texel values required for trilinear interpolation are available simultaneously."[3] The texels are stored in a memory 41'. The memory is divided into two banks, TRAM1 and TRAM2. The system thus

> ensures that arrays T.Li and T.Li+1 for two adjacent
> levels of a given texture pyramid will always be
> stored in different banks TRAM1 and TRAM2.[4]

Williams goes on to disclose a system for simultaneously addressing the memory banks in order to simultaneously access the texels for the two different levels.[5]

Thus, both Williams and Schilling are directed to arrangements wherein data from two mip-map levels are accessed to provide the data necessary for the trilinear interpolation.

The above assemblies are not the same as the invention of Claims 10 and 14. Claim 10 specifically recites that there is a lower level mip-map generator that generates the next below level mip-map data based on mip-map data for the selected mip-map level in the cache. Claim 14 recites the step of performing this data generation based on the mip-map data for the selected mip-map level that is stored in the cache.

The claimed invention eliminates the need to provide the duplicative components of the prior art. The processing steps needed to facilitate the simultaneous retrieval of mip-map date for plural mip-map levels are likewise eliminated. Therefore, Applicant's invention as recited by Claims 10 and 14 is both not suggested by the prior art and has advantages that are not present in the prior art. Therefore, these claims are directed to an invention that is patentably distinct over the prior art.

In the Office Action, Fowler was cited for being relevant to independent Claims 8 and 9 and some of the claims dependent

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[3] GB 2 240 016 A, page 14, lines 23-25.
[4] GB 2 240 016 A, page 14, lines 26-30.
[5] GB 2 240 016 A, page 18, line 19 to page 19, line 11.

from Claim 10. This patent has a filing date of July 16, 1999. This date is *after* the November 6, 1998 filing date of United Kingdom Patent Application No. 9824407.2, the application from which this Application claims priority.

The above priority claim was set forth in the Applicant's Declaration submitted when this application was nationalized. It is stated in the Office Action that the Patent and Trademark Office received a certified copy of the '407.2 GB Application. Therefore, it is submitted that the Applicant has perfected its November 6, 1998 priority date for this application under 35 U.S.C. Sec. 119. Fowler therefore should not be applied as a reference against this application.

The dependent claims are all allowable at least because they depend from allowable independent claims.

Moreover, Claims 3, 13 and 21 are directed to the system and method of this invention wherein the lower level mip-map data are based on the decompressed mip-map data for the selected mip-map level. Claims 17-21 are directed to the version of the invention wherein a plurality of decompression means-filter pairs both decompress the selected mip-map level mip-map data and generate the lower level mip-map data.

There is no suggestion of the above assemblies in the cited prior art. Therefore, at least these claims are further in condition for allowance because they are independently directed to a patentable invention.

In conclusion, it is submitted that all of the claims of this application are directed to a patentable invention and are in an allowable form. Since the claims and the other parts of this application are in an allowable state, the

Applicant now courteously requests prompt issuance of a Notice of Allowance.

Respectfully submitted,

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